UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/903,245	07/11/2001	Debra M. Bell	303.751US1	9496

7590 06/29/2005

Schwegman, Lundberg, Woessner & Kluth, P.A.
Att: Daniel J. Kluth
P.O. Box 2938
Minneapolis, MN 55402

EXAMINER	
WONG, LINDA	

ART UNIT	PAPER NUMBER
2634	

DATE MAILED: 06/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/903,245	BELL, DEBRA M.	
	Examiner	Art Unit	
	Linda Wong	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 February 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *24 and 32* is/are allowed.

6)☒ Claim(s) *1-14 and 18-44* is/are rejected.

7)☒ Claim(s) *15-17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 February 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-44 have been considered but are moot in view of the new ground(s) of rejection.

Claim Objections

2. **Claim 16** recites the limitation "the number of delay stages" in claim 13. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. **Claims 7,11,13,23,24,31,32** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 11 recites a logic circuit receiving the shifting signals and the select signal. Based on the diagram and specification, page 7, lines 16-24, the logic circuit receives the shifting signals, but the phase detector receives the selected signal. The logic circuit recited in claims 7,11,13,23,24,31,32 will be considered as described in the specification and diagrams.

Claim Rejections - 35 USC § 102

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. **Claims 1,2,3** are rejected under 35 U.S.C. 102(e) as being anticipated by Kondo (US Patent No.: 6297680).

   a. **Claim 1**, Kondo discloses a coarse delay segment (Fig. 2), a fine delay segment connected to the coarse delay segment for applying a fine delay (Fig. 3 and Fig. 1, labels 300 and 301), wherein the fine delay segment is configured for adjusting a fine delay based on a plurality of shifting signals (Fig. 1, labels 303 and 301) and wherein the coarse delay is configured for adjusting the coarse delay based on a combination of the shifting signals and the fine delay (Fig. 1, label 303, 300,301,FEEDBACK CLOCK).

   b. **Claim 2**, Kondo discloses the fine delay is less than the coarse delay. (Col. 3, lines 47-50).

   c. **Claim 3**, Kondo discloses the fine delay is less than the coarse delay, which indicates that the largest fine delay is smaller than the smallest delay of the coarse delay.

5. **Claims 42-44** are rejected under 35 U.S.C. 102(e) as being anticipated by Baker et al (US Patent No.: 6445231).

   a. Regarding **claim 42**, Baker et al disclose a coarse delay segment (coarse loop Fig. 2A, Label 205a) that applies a coarse delay (Col. 3, lines 52-53), a fine delay segment that applies a fine delay (Col. 3, lines 54-55), both comprised of a plurality of coarse and

fine delay signals, respectively (fine loop fig. 2A, label 205b and Fig. 9, label 910), a feedback from the fine delay that is adjusted by the coarse delay segment (Fig. 2A), a shift register that controls and selects the next delay or output (Col. 4, lines 60-61), a phase detector that generates a difference in phase between *9 inputs, and the shift register detects when to adjust the coarse and fine delay segments accordingly. (Fig. 5A)

b. Regarding **claim 43**, Baker et al disclose a coarse delay segment (Fig. 2A, label 205a) provides wide frequency lock range and a fine delay segment that provides tight locking. (Col. 1, lines 64-67 and Col. 2, lines 1-2)

c. Regarding **claim 44**, Baker et al disclose a shift register receiving inputs from a phase detector and based on the signals from the phase detector, the shift register controls and selects the next delayed signal. (Fig. 9 and Col. 8,lines 1 5-34)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. **Claims 4,5,6** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kondo (US Patent No.: 6297680) in view of Keeth et al (US Patent No.: 6101197).

a. **Claims 4 and 5** are rejected as stated in the previous non-final rejection. Although Kondo does not disclose how the coarse and fine delays are adjusted, Keeth et al

disclose a coarse delay (within coarse delay circuit Fig 2, label 158) adjusted "whenever the maximum or minimum delay of the fine delay circuit" is reached. (Abstract, lines 12-14) Keeth et al also disclose that the coarse delay is decreased when the fine delay circuit within the range of the predetermined fine delay minimum and increased when the fine delay segment is within the range of the predetermined maximum. (Col. 5, lines 9-17) By adjusting the coarse delay and fine delay, it would be obvious to one skilled in the art to use this method to provide better synchronization.

b. **Claim 6** inherits all the limitations of claims 4 and 5.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. **Claims 7,8,10-14** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kondo (US Patent No.: 6297680) in view of Oh (US Patent No.: 6765976).

a. **Claim 7**, Kondo discloses a coarse delay segment (Fig. 1, label 300), a fine delay segment connected to the coarse delay segment (Fig. 1, labels 301 and CLKf), wherein the fine delay includes a selector, responsive to a select signal (Fig. 3, labels CONTROL SIGNAL ϕCTL, ϕ2 and ϕ3) for selecting a fine delay amount the fine delay signals (Fig. 3, labels TAPL1-3, TAP0 and TAPR1-3 and Col. 4, lines 38-47) to generate an internal clock (Fig. 3, label INTERNAL CLOCK), a phase detector (Fig. 1,

label 302) for generating a plurality of shifting signals (Fig. 1, label 303) based on a phase difference (Fig. 1, label DECTED SIGNAL), wherein the fine delay segment provides a selected signal based on the plurality of shifted signals (Fig. 1, labels ϕCTL, ϕ2 and Col. 4, lines 38-56). Although Kondo does not disclose a logic circuit, Oh discloses a logic circuit (Fig. 5, label 356) responsive to the combination of the plurality of shifting signals (Fig. 1, label SL and SR) and select signal (Fig. 1, label OUT_CLK1) to enable coarse delay adjustments (Fig. 1, label SL, SR and 102). It would be obvious to one skilled in the art to incorporate the phase detector, comprising a logic circuit, disclosed in Oh's invention with Kondo's invention to provide indication of whether to stop the coarse delay from tuning so to prevent unnecessary adjustment when the clocks are found to be synchronized. (Col. 4, lines 32-35)

b. **Claim 8**, Kondo discloses a fine delay segment with an adjustable range. (Fig. 4, Col. 4, lines 57-67 and Col. 5, lines 1-3).

c. **Claim 10**, Kondo discloses a coarse segment including a delay line (Fig. 1, label 300 and Fig. 2) and a controller causing the delay line to adjust the coarse delay based on the shifted signals and select signal (Fig. 2, labels ϕCTL, ϕ2, ϕ3 and Col. 4, lines 15-31)

d. **Claim 11** inherits all the limitations of claim 7, but claim 7 does not recite a logic circuit and a fine delay segment as recited in claim 11. Kondo discloses a coarse segment comprised of a plurality of delay stages (Fig. 2), a controller enabling the delay line to adjust the coarse delay based on the shifting signals and the selected signal (Fig. 2, labels ϕCTL, ϕ2, ϕ3 and Col. 4, lines 15-31 and Fig. 1, label INTERNAL CLOCK), a fine delay segment including a plurality of fine delays (Fig. 3), a selector (Fig. 3, labels CONTROL SIGNAL ϕCTL, ϕ2 and ϕ3) and a shift register connected to the phase detector and selector (Fig. 1, labels 303, ϕCTL, ϕ2, ϕ3 and 300), the shift register

receiving the shifting signals to activate the select signal (Fig. 3, labels ϕCTL, ϕ2, ϕ3), wherein the selects the internal clock signal based on the activated select signal. (Fig. 3, labels TAPL1-3, TAP0 and TAPR1-3 and Col. 4, lines 38-47) Although Kondo does not disclose a logic circuit, Oh discloses a logic circuit (Fig. 5, label 356) responsive to the combination of the plurality of shifting signals (Fig. 1, label SL and SR) and select signal (Fig. 1, label OUT_CLK1) to enable coarse delay adjustments (Fig. 1, label SL, SR and 102). Since the logic circuit disclosed by Oh is connected to the phase detector and the phase detector, disclosed by Kondo, is connected to the coarse delay, it would be obvious to one skilled in the art to replace the phase comparator found in Kondo's invention with Oh's phase detector connected to the logic circuit to provide indication of whether to stop the coarse delay from tuning so to prevent unnecessary adjustment when the clocks are found to be synchronized. (Col. 4, lines 32-35)

e. **Claim 12** inherits all the limitations of claim 2.

f. **Claim 13** inherits all the limitations of claim 11, but claim 11 does not recite a controller. Kondo discloses a controller (Fig. 2, label 401) to receive coarse adjust signals (Fig. 2, labels ϕCTL, ϕ2, ϕ3) to adjust the coarse delay, wherein the coarse controller adjust the coarse delay (Fig. 2, labels 411, TAP1-n) and inherently discloses a selector (Fig. 3, label 501) selects the fine delay until the clocks are synchronized. (Fig. 1, label FEEDBACK CLOCK).

g. **Claim 14** inherits all the limitations of claim 2.

8. **Claim 9** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kondo (US Patent No.: 6297680) in view of Oh (US Patent No.: 6765976) and further in view of Keeth et al (US Patent No.: 6101197).

a. Regarding **claim 9**, as explained in the rejection of claim 8, Keeth et al indicates an adjustment of coarse delay range and fine delay range in the coarse delay circuit and fine delay circuit. (Abstract, lines 12 -14)

9. **Claims 18,20-22,28,30-31,33** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kondo (US Patent No.: 6297680) in view of Baker et al (US Patent No.: 6445231).

a. Regarding **claim 18**, Baker et al disclose a main memory containing plurality of memory cells and an output circuit connected to the main memory. (Col. 3, lines 11-23) A DLL connected to the output circuit. Claim 1 encloses the limitations of the DLL. (Col. 3, lines 31-35)

b. Regarding **claims 20 and 21**, Baker et al disclose a data bus connected to the output circuit and main memory, comprised of memory cells. (Col. 3, lines 21-23 and lines 12-19) In Fig. 2a, Baker et al shows the DLLout as an input (Fig. 2A, label 212) to the output circuit. The CLKout, equivalent to DS, is synchronized with the data signal, DQ. (Col. 4, lines 8-10) Baker et al depicts in Fig. 2A, an external clock, CLKin, which is synchronized to CLKout, the output from the DLL and output model. The data signal, DQ, is synchronized with DS, which inherently indicates that the external clock is synchronized with the data signal. (Co1. 4, lines 8-30)

c. Regarding **claim 22**, Baker et al disclose a model circuit that is "identical to output circuit". (Col. 4, lines 3-4) As depicted in Fig. 2A, the model circuit (output model Fig. 2A, label 216) is connected to the fine delay segment (fine loop Fig 2A, label 205b).

d. Regarding **claim 28**, Baker et al include a processor connected to the memory device and inherit all the limitations of claim 18. (Col. 10, lines 7-8)

e. Regarding **claim 30**, Baker et al disclose a data bus connected between the processor and the memory device and inherits all the limitations of claim 21. (Col. 10, lines 7-8)

f. Regarding **claim 31**, Baker et al teach a processor connected to the memory device, which comprises of a plurality of memory cells, and inherits all the limitations of claim 18. (Col. 10, lines 7- 8)

g. Regarding **claim 33**, Baker et al include a data bus connected between the processor and the memory device (Fig. 15) and inherit all the limitations of claim 21.

10. **Claims 19,29** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kondo (US Patent No.: 6297680) in view of Baker et al (US Patent No.: 6445231) and further in view of Keeth et al (US Patent No.: 6101197).

a. **Claim 19** inherits all the limitations of claims 4 and 5.

b. **Claim 29** inherits all the limitations of claims 4 and 5.

11. **Claims 23,25-27** are rejected under 35 U.S.C. 103(a) as being unpatentable over Baker et al (US Patent No.: 6445231) in view of Kondo (US Patent No.: 6297680) and further in view of Oh (US Patent No.: 6765976)

c. Regarding **claim 23**, Baker et al (US Patent No: 6445231) disclose a main memory with plurality of memory cells along with an output circuit connected to the memory cell. (Col. 3, lines 8-30) Claim 7 encloses all the limitations of the DLL claimed.

d. **Claim 25** inherits all the limitations of claim 21.

e. **Claim 26** inherits all the limitations of claim 21.

f. **Claim 27** inherits all the limitations of claim 22.

12. **Claim 34** is rejected under 35 U.S.C. 103(a) as being unpatentable over Baker et al (US Patent No.: 6445231) in view of Keeth et al (US Patent No.: 6101197).

    a. Regarding **claim 34**, Baker et al depict a clock input delayed by a coarse delay in the coarse delay segment (Fig. 2A, label 205a), fine delay segment receiving an input from the coarse delay segment to output a fine delayed signal (Fig. 2A, label 211), a shifting register controlled by the output of the phase detector, which detects the difference between CLKin and CLKout (Fig. 3A), a register controller, which controls the shifting of the delay line of the coarse and fine delay (Fig. 5A). Although Baker et al does not disclose that the coarse delay is shifted based on the fine delay, Keeth et al disclose that the coarse delay is shifted when the fine delay has reached a predetermined maximum or minimum. (Col. 5, lines 9-17)

13. **Claim 35** is rejected under 35 U.S.C. 103(a) as being unpatentable over Baker et al (US Patent No.: 6445231) in view of Keeth et al (US Patent No.: 6101197), further in view of Kondo (US Patent No.: 6297680) and further in view of Oh (US Patent No.: 6765976)

    a. **Claim 35** inherits all the limitations of claim 7.

14. **Claims 36-41** are rejected under 35 U.S.C. 103(a) as being unpatentable over Baker et al (US Patent No.: 6445231) in view of Keeth et al (US Patent No.: 6101197), further in view of Kondo (US Patent No.: 6297680).

    a. **Claim 36** inherits all the limitations of claim 2.

    b. **Claim 37** inherits all the limitations of claim 3.

    c. **Claim 38** encloses all the limitations of claim 3.

    d. **Claim 39** inherits all the limitations of claim 6.

e. **Claim 40** inherits all the limitations of claims 4 and 5.

f. **Claim 41** inherits all the limitations of claims 4 and 5.

Allowable Subject Matter

7. **Claims 15,16,17** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claim 16 must be amended to overcome the lack of antecedent objection.

8. **Claim 24,32** is allowed over prior art.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linda Wong whose telephone number is 571-272-6044. The examiner can normally be reached on 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on (571) 272-3056. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LW

STEPHEN CHIN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600